ABSTRACT OF THE DISCLOSURE

A delay locked loop (DLL) circuit having a duty cycle corrector (DCC) that has a broad range of duty cycle correction, consumes only a small amount of power, has few restrictions on operating frequency, and improves the characteristics of a memory device is described. The delay locked loop circuit includes an additional loop for duty cycle correction as well as loops for controlling a rising edge and a falling edge of output signals. Thus, the delay locked loop circuit can internally correct the duty cycle without the use of a phase blender.